IN THE CLAIMS:

Claims 1-36 and 40-51 have been cancelled. Claims 37-39 and 52-54 have been amended herein. All of the pending claims are presented below. This listing of claims will replace all prior versions and listings in the application. Please enter these claims as amended.

Listing of the Claims:

1.-36. (Cancelled)

37. (Currently amended) A method of preventing a circuit having a teat mode entry function from entering a subsequent test mode after ~~said~~ the circuit enters a first test mode, comprising:

initiating a test mode blocking signal after ~~said~~ the circuit completes ~~said~~ the first test mode; and

exclusively controlling ~~said~~ the test mode entry function of ~~said~~ the circuit with ~~said~~ the test mode blocking signal.

38. (Currently amended) The method in claim 37, further comprising generating ~~said~~ the test mode blocking signal responsive to a final test latch of ~~said~~ the circuit dining ~~said~~ the first test mode.

39. (Currently amended) The method in claim 38, further comprising originating ~~said~~ the test mode blocking signal from ~~said~~ the circuit.

40.-51. (Cancelled)

52.   (Currently amended) A method of protecting a test circuit from receiving a subsequent latching signal after receiving at least one prior latching signal, comprising:

allowing at least one prior latching signal to reach ~~said~~ the test circuit;

performing a test circuit operation for each prior latching signal;

providing a lockout signal; and

stopping any subsequent latching signal with ~~said~~ the lockout signal.

53.   (Currently amended) The method in claim 52, wherein providing ~~said~~ the lockout signal further comprises generating ~~said~~ the lockout signal responsive to a last prior latching signal.

54.   (Currently amended) A method of preventing a test vector decode circuit from reentering a test mode, comprising:

making a reentry into ~~said~~ the test mode dependent upon a change of an output vector of ~~said~~ the test vector decode circuit; and

making ~~said~~ the change of ~~said~~ the output vector dependent upon ~~said~~ the reentry into ~~said~~ the test mode.